CLAIMS

What is claimed as new and desired to be secured by letters patent of the United States is::

1. A semiconductor manufacturing apparatus, comprising:

a substrate holding unit for holding a semiconductor wafer substrate;

a discharging mechanism for discharging droplets of raw etching barrier resin through at least one discharging nozzle onto a first surface of said semiconductor wafer substrate held on said substrate holding unit;

a drive mechanism for displacing at least one of said semiconductor wafer substrate and said discharging nozzle; and

a control unit for controlling said discharging mechanism and said drive mechanism such that said raw etching barrier resin is attached to said first surface of said semiconductor wafer substrate, wherein

said semiconductor wafer substrate includes a plurality of fuse elements and a dielectric layer having openings corresponding to a location for forming said plurality of fuse elements, and wherein

said control unit controls such that said raw etching barrier resin is discharged into an opening corresponding to a location of at least one of said plurality of fuse elements.

2. The semiconductor manufacturing apparatus according to claim 1, wherein:

said discharging mechanism includes a plurality of discharging nozzles.

3. The semiconductor manufacturing apparatus according to claim 1, wherein:

said substrate holding unit includes a substrate temperature control mechanism for controlling a temperature of said semiconductor wafer substrate.

4. The semiconductor manufacturing apparatus according to claim 1, further comprising:

a second discharging mechanism, wherein the first and second discharging mechanism discharge different amounts of said raw etching barrier resin.

5. The semiconductor manufacturing apparatus according to claim 4, wherein:

said control unit controls said first and second discharging mechanism, and said drive mechanism, such that the first discharging mechanisms discharges droplets of said etching barrier resin of an amount smaller than the second discharging mechanism into an area near a vicinity of a periphery of said opening.

6. The semiconductor manufacturing apparatus according to claim 1, wherein:

said discharging mechanism includes a resin temperature control mechanism for controlling a temperature of said raw etching barrier resin contained in a resin container unit.

7. A method for manufacturing a semiconductor device, comprising:

selectively disconnecting at least one of a plurality of fuse elements formed on a semiconductor wafer substrate, said semiconductor wafer substrate having a dielectric layer with a plurality of openings that correspond to locations for forming said plurality of fuse element;

forming a layer of etching barrier resin in an opening corresponding to a location of at least one fuse element not to be selectively disconnected out of said plurality of fuse elements; and

implementing either one of dry and wet etching steps using said layer of etching barrier resin as a mask such that at least one fuse element not to be selectively disconnected is without a corresponding overlying layer of etching barrier resin, and said fuse element selected to be disconnected is etched.

8. The method for manufacturing a semiconductor device according to claim 7, wherein

the step of forming said layer of etching barrier resin comprises:

scanning at least one discharging nozzle for discharging said raw etching barrier resin while discharging droplets of said raw etching barrier resin so as to replenish said opening corresponding to said location of said fuse element not selectively disconnected, and

hardening said raw etching barrier resin.

9. The method for manufacturing a semiconductor device according to claim 8, wherein:

the forming of said layer of etching barrier resin includes discharging droplets of said raw etching barrier resin of an amount smaller for an area in vicinity of a periphery, than other portions, of said opening.

10. The method for manufacturing a semiconductor device according to claim 7, wherein said plurality of fuse elements are formed from polysilicon.

11. A semiconductor device, comprising:

a plurality of fuse elements formed on a first surface of a semiconductor wafer substrate, wherein at least one of said plurality of fuse elements is selected for disconnection; and

a dielectric layer having at least one opening corresponding to a location for forming said at least one fuse element, wherein a layer of etching barrier resin is formed in an opening in said dielectric layer corresponding to a location of a fuse element not to be disconnected but not in a further opening corresponding to a location of a further fuse element selected to be disconnected.

12. A semiconductor device, comprising:

a dividing resistor component including at least two resistors having a resistive value, said dividing resistor component being capable of providing an output

voltage by dividing an input voltage by said resistive value and of adjusting said output voltage by selectively disconnecting a fuse element in said semiconductor device, wherein a dielectric layer is formed having at least one opening corresponding to a location for forming at least one fuse element, and wherein

a layer of etching barrier resin is formed in an opening in said dielectric layer corresponding to a location of a fuse element that is not selectively disconnected out of said at least one fuse element, but not in a further opening corresponding to a location of a further fuse element selectively disconnected.

13. A semiconductor device, comprising:

a plurality of dividing resistors having a resistive value for supplying a divided voltage generated by dividing an input voltage by said resistive value;

a reference voltage generator for supplying a reference voltage; and

a comparator circuit for comparing said divided voltage with said reference voltage, wherein said plurality of dividing resistors include at least two resistors, which are capable of generating an output voltage by dividing an input voltage by said at least two resistors and adjusting said output voltage by disconnecting a fuse element in said semiconductor device.

14. A semiconductor device, comprising:

an output driver for controlling an output of an input voltage;

a plurality of dividing resistors having a resistive value for supplying a divided voltage by dividing an output voltage by said resistive value;

a reference voltage generator for supplying a reference voltage;

a comparator circuit for comparing said divided voltage with said reference voltage to control an operation of said output driver based on comparison results,

wherein said dividing resistors comprise a dividing resistor component, including at least two resistors, which are capable of providing an output voltage by dividing an input voltage by said at least two resistors and adjusting said output voltage by disconnecting a fuse element in said semiconductor device.

15. A semiconductor manufacturing apparatus, comprising:

substrate holding means for holding a semiconductor wafer substrate;

first discharging means for discharging droplets of raw etching barrier resin through at least one discharging nozzle means onto a first surface of said semiconductor wafer substrate held on said substrate holding means;

drive means for displacing at least one of said semiconductor wafer substrate and said discharging nozzle means; and

control means for controlling said first discharging means and said drive means such that said raw etching barrier resin is attached to said first surface of said semiconductor wafer substrate, wherein said semiconductor wafer substrate has a plurality of fuse elements and a dielectric layer having openings corresponding to a location for forming said plurality of fuse elements, and wherein said control means controls the discharge of raw etching barrier resin into an opening corresponding to a location of a fuse element that is selected not to be disconnected out of said plurality of fuse elements.

16. The semiconductor manufacturing apparatus according to claim 15, wherein:

said first discharging means includes a plurality of discharging nozzle means.

17. The semiconductor manufacturing apparatus according to claim 15, wherein said substrate holding means is provided with a substrate temperature control means for controlling a temperature of said semiconductor wafer substrate.

18. The semiconductor manufacturing apparatus according to claim 15, further comprising a second discharging means, wherein the first and second discharge means are capable of respectively discharging different amounts of said raw etching barrier resin.

19. The semiconductor manufacturing apparatus according to claim 18, wherein said control means controls said first and second discharging means and said drive means such that a first discharging means discharges droplets of said etching barrier resin of an amount smaller than the second discharging means into an area near a vicinity of a periphery of said opening.

20. The semiconductor manufacturing apparatus according to claim 15, wherein:

said first discharging means is provided with a resin temperature control

means for controlling a temperature of said raw etching barrier resin contained in a resin container means.

21. A semiconductor device, comprising:

a plurality of dividing resistors having a resistive value for supplying a divided voltage by dividing an input voltage by said resistive value;

reference voltage generator means for supplying a reference voltage; and

comparator circuit means for comparing said divided voltage with said reference voltage wherein said plurality of dividing resistors comprises a dividing resistor component, including at least two resistors, which is capable of providing an output voltage by dividing an input voltage by said at least two resistors and adjusting said output voltage by disconnecting a fuse element on the semiconductor device.

22. A semiconductor device, comprising:

output driver means for controlling an output of an input voltage;

a plurality of dividing resistors having a resistive value for supplying a divided voltage by dividing an output voltage by said resistive value;

reference voltage generator means for supplying a reference voltage;

comparator circuit means for comparing said divided voltage with said reference voltage to control an operation of said output driver means based on comparison results, wherein said plurality of dividing resistors comprise a dividing resistor component, including at least two resistors, which is capable of generating an output voltage by dividing an input voltage by said at least two resistors and adjusting said output voltage by disconnecting a fuse elements on the semiconductor device.

23. A semiconductor manufacturing apparatus, comprising:

a semiconductor wafer substrate;

a substrate holding unit for holding said semiconductor wafer substrate;

at least one discharging head for discharging raw etching barrier resin onto a first face of said semiconductor wafer substrate and having at least one discharging nozzle;

a resin container unit connected to said discharging head and containing said raw etching barrier resin;

a drive mechanism for displacing at least one of said semiconductor wafer substrate and said discharging nozzle; and

a control unit for controlling said discharging mechanism and said drive mechanism, wherein said first face of said semiconductor wafer substrate is provided with a plurality fuse element, wherein at least one of said plurality of fuse elements is selected for disconnection, and a dielectric layer having an opening corresponding to a location for forming said at least one fuse element, and wherein said control unit controls said discharging mechanism and said drive mechanism such that said raw etching barrier resin is replenished into an opening corresponding to a location of a fuse element not selected to be disconnected out of said at least one fuse element.

24. The semiconductor manufacturing apparatus according to claim 23, wherein said discharging mechanism is provided with a plurality of discharging nozzles.

25. The semiconductor manufacturing apparatus according to claim 23, wherein said substrate holding unit is provided with a substrate temperature control mechanism for controlling temperature of at least said semiconductor wafer substrate.

26. The semiconductor manufacturing apparatus according to claim 23, wherein each discharge head discharges different amounts of said raw etching barrier resin.

27. The semiconductor manufacturing apparatus according to claim 26, wherein said control unit controls each discharging head and said drive mechanism such that a first discharging head is capable of discharging droplets of said etching barrier resin of an amount smaller than other discharging mechanisms into an area in a vicinity of a periphery of said opening.

28. The semiconductor manufacturing apparatus according to claim 23, wherein said discharging head is provided with a resin temperature control mechanism for controlling a temperature said raw etching barrier resin contained in said resin container unit.